# On the Stability of Millimeter-Wave Power Amplifiers

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***Abstract*** **— In this paper, we discuss issues affecting high-frequency power amplifier stability. K-factor stability will be discussed, with particular emphasis on very high frequency operation, as well as odd-mode push-pull analysis. Both methods will be used to predict the occurrence of millimeter-wave oscillations (Ka-band and above) in high millimeter-wave W-band power amplifiers. We present experimental results confirming the simulation data, and discuss how the methods may be applied to eliminate instabilities in MMIC power amplifiers.**

## I. Introduction

Millimeter-wave power amplifiers are increasingly in demand for higher bandwidth communication, local oscillator sources, automotive radar, and fiber optic communication [1,2]. As the need for higher frequency power amplifiers increases, some design issues affecting power amplifier stability become important. Issues affecting power amplifiers for wireless communications are similar, but given the frequencies involved, a wireless chip with stability problems may be treated with off-chip networks. In the case of a 100 GHz MMIC power amplifier, oscillations which occur at < 500 MHz may be easily treated off-chip with proper terminations, but oscillations occurring at 10-50 GHz must be corrected with a new MMIC design and costly fabrication run. In this paper, we outline stability analysis applied to W-band (75-110 GHz) MMIC power amplifiers, and give some general rules of thumb for designing for amplifier stability out of band.

Often, instabilities in amplifiers can be lived with, and if they are of small-amplitude, may be tolerated. However, with increasing interest in satellite communications or spacecraft flight of MMIC chips and possibilities of sub-room-temperature operation, even in space-craft ambient temperature (100-200 K) (where transconductances and gain can increase), reliability and lifetime are critical performance issues and oscillations must be eliminated.

## II. MMIC Power Combining

In Figure 1 we show a 71-84 GHz MMIC power amplifier, which was previously reported in [1], fabricated by TRW using a 0.1 μm GaAs PHEMT process. The design topology makes use of 4-way and 8-way microstrip power combiners to combine the FETs. The chip photograph and the 4-way combiner is shown in Figure 1. The combiner utilizes odd-mode suppression resistors placed between the FETs. This type of cell is common for combining large devices in parallel to achieve more power.

While we have previously reported the in-band results for this amplifier on-wafer, when we packaged the chip in a waveguide module, we observed some oscillation phenomenon which was difficult to control with off-chip stabilizing networks. The oscillation behavior was transient, and disappeared if we biased the amplifier at Vd =3 V, rather than Vd=2-2.5 V. The behavior, while we could work around it, warranted further investigation.

We tested the amplifier chip with a spectrum analyzer, using GGB industries wafer probes at the input and output of the chip, and applied DC bias with DC needle probes. The output RF probe was attached to a 2.4 mm coaxial cable and fed into a DC-40 GHz spectrum analyzer. We observed that a transient oscillation was present between 32-34 GHz, for drain voltatges up to 2.9 V, and Vg from -.5 V to +.1V, but that the oscillation disappeared for Vd>2.9 V. The spectrum with the 34

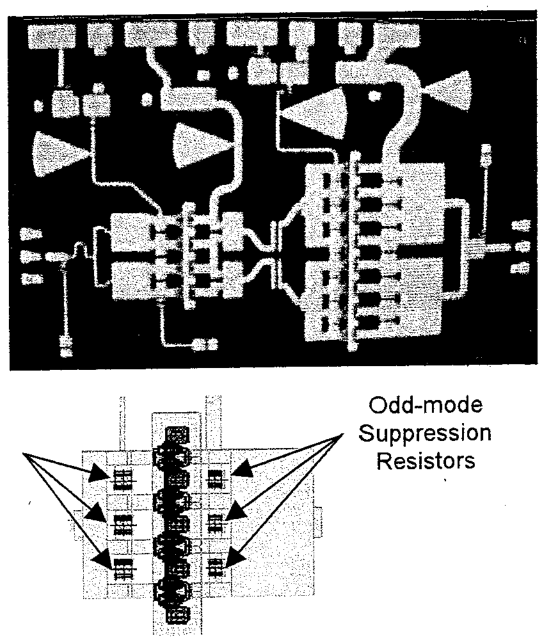



Figure 1 Top: Chip photograph of two-stage amplifier to be analyzed. Bottom: Typical power-combining cell for 4-way power combining of FETs, showing odd-mode suppresion resistors between each FET at the gate and drain sides.

GHz peak is shown in Figure 2, for Vd=1.5 V, Vg=-0.3 V, and Id= 190 mA. The peak varied from 32-34 GHz depending on Vg. Our investigation into the nature of the oscillation revealed that it was convincingly coming from the second stage of the MMIC chip (it remained whether stage 1 was turned on or off), and occurred for no applied RF signal (only DC bias). It was not dependent on whether the input was terminated or left open. This work describes the analysis we have performed on the MMIC design into the nature of the oscillation, and the methods we have used to correct the oscillation. These methods can be applied to all types of high frequency MMIC amplifiers to guarantee stability in a MMIC design.

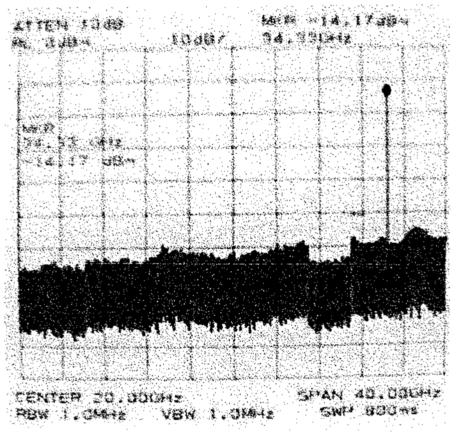


Fig. 2. Spectrum of chip showing 34 GHz oscillation.

## III. Methods of Stability Analysis

Two-port small-signal simulations of the amplifier chip between the RF input and RF output revealed no special anomalies between 0-150 GHz, while the in-band stability factor, *K*, was greater than 2 between 60-85 GHz. A value of *K*>1 guarantees unconditional stability. We therefore investigated two other ways to simulate the circuit, to make the experimentally-verified oscillation at 32-34 GHz appear in the simulations.

We have performed two types of stability analyses in this work. We focused our simulations on the second stage of the chip, since experimentally it appeared responsible for the oscillation. First, we performed a *K*-factor analysis of the bias lines in each stage of the amplifier chip, as shown in Figure 3, according to reference [3]. The input and output of the circuit are terminated in 50 Ohms, while ports are inserted at the input to the bias lines of the circuit. Port 1 is applied to the gate bias line while Port 2 is applied to the drain bias line. The figure illustrates this for the bias-line analysis of the second stage. This method is usually applied to low frequency oscillations < 2 GHz, but it is equally applicable to higher frequencies as well.

Figure 4 illustrates the *K*-factor calculated between the gate and drain bias lines of the APH351 power amplifier chip, with the chip input and output terminated in 50 ohm resistors. The nominal value of Gm=100 mS was used for the PHEMT device in simulation. While the *K*-factor is well above 1 over the entire range between 1 and

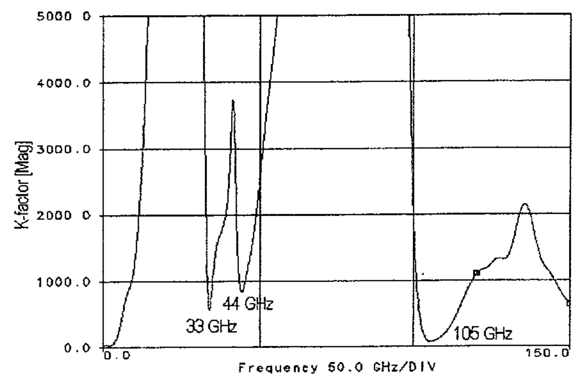



Figure 4. K-factor analysis of MMIC circuit from 0-150

150 GHz, there are several regions which exhibit dips in *K*. The region below 5 GHz is a region of low K-factor, given the high gain these transistors exhibit at low frequencies. However, instabilities can usually be handled with off-chip bias networks to decrease low frequency gain, and we will not address that problem in this work. We will instead focus our attention on the potential regions of instability between X-band and W-band. In particular, sharp dips occur at 33 and 44 GHz, though they are K>500. Additionally, K~100 at 105 GHz. Although there are some potential areas of concern, K>>1 everywhere.

The second method we used to detect the instability in simulations was to apply a push-pull analysis to the second stage of the circuit, shown in Figure 5. In this method, the circuit is broken strategically at a point where the power is to be split into two legs, and an ideal transformer is inserted. The transformer serves to drive

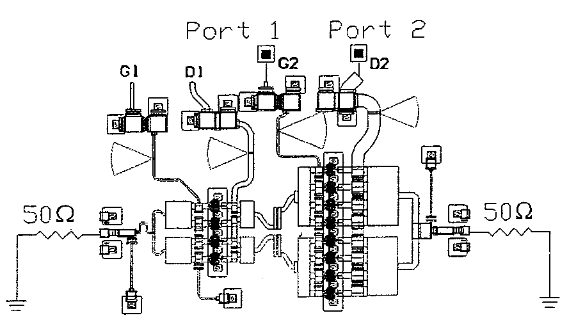



Figure 3. Configuration for simulated K-factor analysis of the second stage bias lines (after Ref 3).

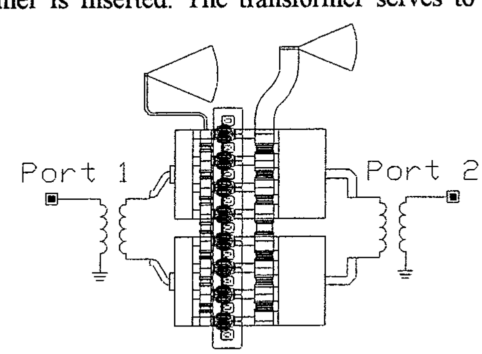



Figure 5. Configuration for simulated push-pull analysis of the second stage of the MMIC power amplifier.

the two legs of the power splitter 180 degrees out of phase, thereby forcing an odd-mode condition [4,5]. The transformer is applied at the input and output of the split circuit. Figure 5 shows the setup of the problem in the linear simulator, and the *K*-factor is calculated between the input and output of *only* stage 2. The bias circuitry above the radial stubs is not shown in the figure, although it is simulated. While the pushpull analysis isolates the second stage from the first, we believe that these two methods of analysis performed together comprise a thorough study of potential stability problems in this type of power amplifier.

In order to make the instability more obvious in the simulations, we enhanced the value of transconductance, Gm, to twice its nominal value, using Gm=0.195 mS for the simulations to follow. Although this is a relatively high value to use, such a theoretical exercise is more likely to make potential instabilities appear, and then correcting the circuit for large variations in Gm will make it more immune to undesired problems. In addition, one could also vary other device parameters in the model to check for instabilities. One possibility is to vary the Cgs and Cgd by 40 % or so, since these parameters also vary with changing bias conditions considerably.

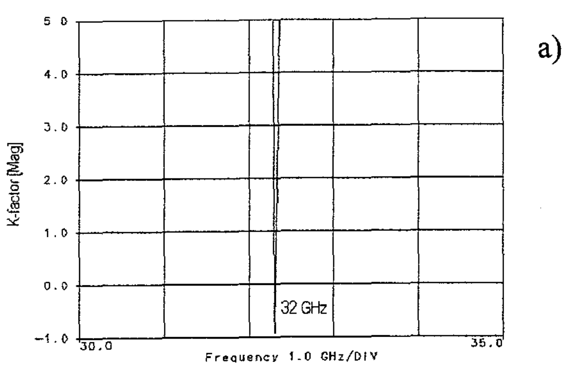
## IV. Simulation Results

First, we applied the bias-line analysis (from Figure 3) to calculate the *K*-factor of the stage 2 bias lines with the enhanced value of Gm. The full spectrum to 150 GHz is not plotted here, however, we observed that the *K*-factor appeared relatively benign *except* in the region of 30-35 GHz. In this area, a sharp dip in *K*-factor was observed around 32.8 GHz, indeed, at one of the experimentally *measured* frequencies. The plot is shown in Figure 6a.

Figure 6b shows the results of a push-pull analysis (from Figure 5) on the second stage of the same chip. A sharp spike in *K*-factor at 32.5 GHz is also observed. Our analysis has shown that a dip in *K*-factor appeared at 32-33 GHz in both simulations, in agreement with the experimentally identified oscillation between 32-34 GHz, and despite the fact that $K>1$ everywhere in the simulation data of the whole chip from RF input to RF output.

## V. Elimination of Undesired Oscillations

With sensitive simulations it is possible to trace the cause of the Ka-Band oscillation and remedy it. We have found that the oscillation was due to an improper value of odd-mode resistors, as well as placement of the odd-mode resistors too far away from the PHEMTs (see Figure 1). By judiciously choosing the odd-mode resistor value to more closely match the input impedance of the PHEMT (~5 Ohms), we were able to eliminate the oscillation conditon in simulation. The optimum value of odd-mode resistor was found to be 10 Ohms, and it had to be placed



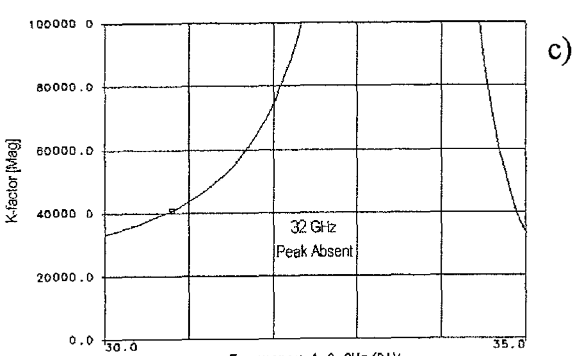
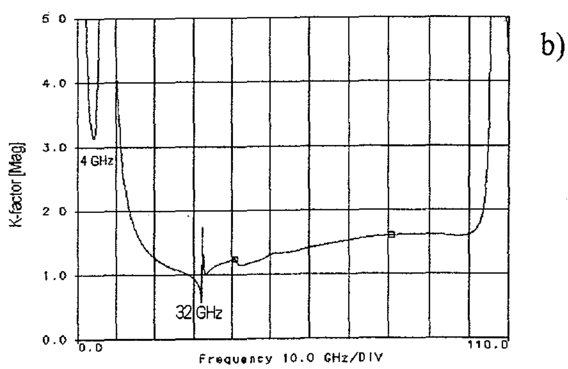




Figure 6a.(Top) Simulation of the *K*-factor between the gate and drain bias lines of stage 2; 6c(Bottom): Simulation of the *K*-factor between the gate and drain bias lines after decreasing the value of odd-mode suppression resistors and moving the resistors closer to the fets. Gm= 195 mS. Note the scale of *K* (0 to 100000).



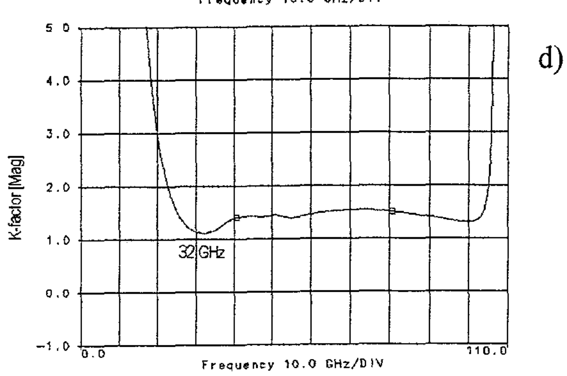




Figure 6b (Top) Simulation of k-factor of pushpull analysis of stage 2; 6d(Bottom): Simulation of *K*-factor in pushpull analysis of stage 2, after decreasing the value of odd-mode resistors., and moving the resistors closer to the PHEMTs. Gm= 195 mS.

within 40 μms of the PHEMTs in order to be effective. With these changes to the second stage of the circuit, we achieved the simulation data in Figures 6c and 6d. Figure 6c shows the bias-line analysis and Figure 6d shows the push-pull analysis, with R=10 Ohms instead of 50 Ohms, and with the odd-mode resistors placed 10 μm closer to the PHEMTs. In both cases, the potential region of instability has disappeared, and has not reappeared at any other frequency. We next present experimental data on the redesigned amplifier chip, showing that the instability has indeed been eliminated up to 40 GHz.

## III. Experimental Results

The MMIC chip was redesigned according to the simulations, to have smaller-valued odd-mode resistors, and fabricated alongside the orginal chip design. Two types of data were obtained for the stability measurements: spectrum analyzer data up to 40 GHz., and small-signal S-parameters. S-parameters were obtained using an HP 8510A vector network analyzer with Oleson Microwave Labs extension modules covering WR15 (50-79 GHz). All of the data were obtained via on-wafer measurements with RF wafer probes. DC power was applied to the chips using needle probes for gate and drain bias.

While Figure 2 showed the 34 GHz oscillation in the original circuit, Figure 7 illustrates the clean spectrum obtained from the redesigned MMIC. No oscillation at 32-34 GHz was observed in the new circuit under any bias condition. As in Figure 2, Vd=1.5 V, and Vg=-.3 V.

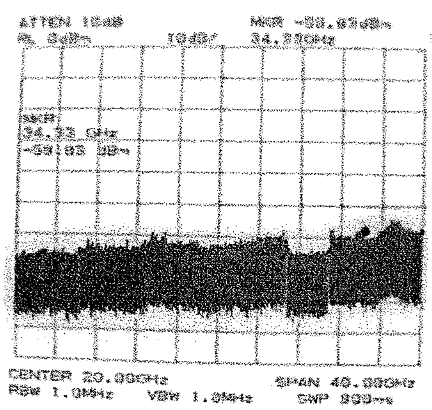


Figure 7. Spectrum of redesigned amplifier chip, showing elimination of the 34 GHz oscillation at all bias conditions.

Small signal V-band S21 measurements of the original circuit and the redesigned, "fixed" circuit are shown in Figure 8. The original circuit exhibits a spike in the S21 data at 67 GHz, 2x (33.5 GHz). We believe this to be the second harmonic of the 32-34 GHz oscillation. The "fixed" circuit exhibits no such spike, and also has about 2 dB higher gain since the oscillation has been eliminated. Gain and drain current were suppressed in the original circuit due to the oscillation.

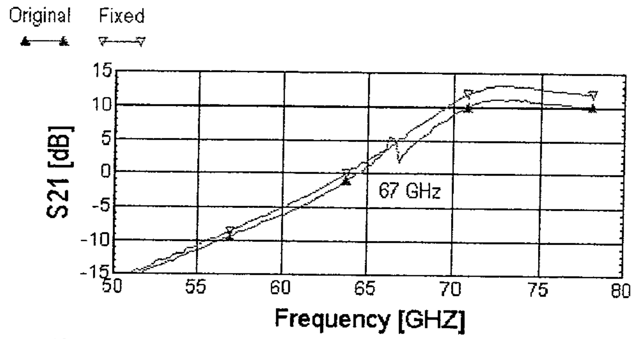



Figure 8. V-band S21 measurements of original chip (dark triangles), showing gain spike at the second harmonic of 33 GHz, and the "fixed" chip (light triangles), with no spike. Gain is also enhanced in the fixed chip.

## VI. Conclusion

We conclude by stressing that stability analysis in the band of interest is insufficient to guarantee stable operation for very high frequency MMIC amplifiers. Out of band stability must be analyzed, especially in the case of power-combined transistors where odd modes are possible. Even when a two-port, input-output *K*-factor analysis may look sufficient to guarantee stability, checking the bias-line stability as well as a push-pull analysis is important in power-combined cells, where several modes are possible. We have outlined two methods for analyzing circuits for stability, as well as indicated parameters which may be varied to make a potential instability appear in simulations, and used these methods to correct an existing instability in Ka-Band which was difficult to detect in conventional simulations. Future work could involve large signal S-parameter measurements and *K*-factor analysis for stability.

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